REMARKS

The Official Action mailed August 6, 2002 has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time.

Applicants note with appreciation the consideration of the Information Disclosure Statements filed on November 12, 1998; December 17, 1998; October 10, 2000; January 3, 2001; March 12, 2001; August 24, 2001; September 24, 2001 and May 13, 2002. A further IDS is submitted herewith and careful review and consideration of this IDS is requested.

Claims 1-25 and 34-41 were pending in the present application. Claim 40 has been canceled, all independent claims 1, 6, 11, 16, 19 and 37 have been amended and new claim 42 has been added to recite additional protection to which Applicants are entitled. Claims 1-25, 34-39 and 42 are now pending in the present application, of which claims 1, 6, 11, 16, 19, 37 and 42 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

Applicants appreciate the Examiner's time in conducting an interview on October 7, 2002. During the interview, the features and advantages of the present invention were discussed and features believed to distinguish the present invention over the prior art of record were reviewed. As discussed in more detail below, the amendments submitted herewith are believed to further distinguish the claims over the prior art and favorable reconsideration in view thereof is requested.

More specifically, all independent claims 1, 6, 11, 16, 19, 37 and new independent claim 42 recite that a distance between the channel forming region and the pair of first regions of said first thin film transistor is greater than that of said second thin film transistor. This new limitation is supported by at least Example 1 (page 12, lines 17-29) in the specification.

The present invention recited in claim 1, for example, is a semiconductor device comprising an active matrix circuit having at least one first thin film transistor formed over a substrate, and a driving circuit having at least one second thin film transistor formed over the substrate for driving said active matrix circuit, each of said first and second transistors comprising, a gate electrode, a gate insulating film adjacent to the

gate electrode, and a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions, wherein the pair of second regions of said second thin film transistor are overlapped with the gate electrode of said second thin film transistor and wherein a distance between the channel forming region and the pair of first regions in said first thin film transistor is greater than that of said second thin film transistor.

Paragraph 1 of the Official Action objects to the drawings under 37 CFR 1.83(a) as lacking every feature of the invention as specified in the claims. In response, a new Figure 9 is submitted herewith together with appropriate amendments to the specification. Figure 9 is based on Fig. 1A and merely illustrates the multilayered gate electrode discussed on page 4 of the specification. No new matter is added and reconsideration of the objections under Rule 83 is requested in view thereof.

Paragraph 3 of the Official Action rejects claims 1-4, 16, 19-22, 37-38 and 41 as anticipated by U.S. Patent 5,323,042 to Matsumoto. It is well established that "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

It appears that Matsumoto discloses, as shown in FIG.1, that a distance between a channel region 21a and low impurity concentration regions 21a and 21b of the thin film transistor for matrix circuit 12 is equal to that of the thin film transistor for peripheral circuit 13. Therefore, since Matsumoto fails to disclose that a distance between the channel forming region and the pair of first regions in the first thin film transistor is greater than that of the second thin film transistor as now recited in the independent claims, Matsumoto cannot anticipate the claims and favorable reconsideration is requested.

Paragraph 5 of the Official Action rejects claims 5 and 23 as obvious based on the combination of Matsumoto and U.S. Patent 5,028,551 to Dohjo et al. It is

respectfully submitted that Dohjo does nothing to overcome the deficiencies noted above with respect to Matsumoto and that claims 5 and 23 are allowable for the same reasons noted above.

Paragraph 6 of the Official Action rejects claims 6-9, 17, 24-25, and 34-35 as obvious based on Matsumoto. Paragraph 7 of the Official Action rejects claims 11-14, 18, 36 and 40 as obvious based the combination of Matsumoto and U.S. Patent 5,412,493 to Kunii et al. As stated in MPEP § 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

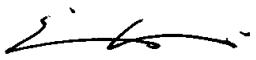
It appears that Kunii et al. disclose a switching element for driving the picture element electrodes having a multi-gate structure and lightly doped drain structure. A length of first and second lightly doped regions 61 and 62 is set to 1μm, the length of third lightly doped region 63 is set to 0.5μm and the length of fourth lightly doped region 64 is set to 1.5μm. Neither Matsumoto nor Kunii, taken alone or in combination, however, disclose or suggest that a distance between the channel forming region and the pair of first regions in a first thin film transistor is greater than that of a second thin film transistor as claimed since Matsumoto does not disclose the length of the low impurity regions. Thus, it is impossible to draw any comparison between the LDD

regions of Matsumoto and Kunii. Therefore, since the prior art of record, taken alone or in combination, fails to teach or suggest each and every limitation of the pending claims, it is submitted that a *prima facie* case of obviousness cannot be maintained and favorable reconsideration is requested.

The remaining rejections set forth in paragraphs 8-10 are also believed to be overcome for the same reasons discussed above and reconsideration is requested based on the above amendments and remarks.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 4, please amend the third full paragraph as follows:

--Referring to Figs. 1A to 1E, a basic process for fabricating a TFT according to the present invention is described below. A base insulating film 102 is formed on a substrate 101. An active layer 103 is formed from a crystalline semiconductor (a semiconductor comprising a crystal even at a small quantity, for example, a single crystal semiconductor, polycrystalline semiconductor, semi-amorphous semiconductor or the like is referred to as "a crystalline semiconductor" in the present invention. An insulating film 104 comprising silicon oxide is formed to cover an active layer 103, and a coating is formed by an anodically oxidizable material. Preferably, an anodically oxidizable material such as aluminum, tantalum, titanium, and silicon, is used as the coating material. Moreover, a monolayered gate electrode using one of the above materials as well as a multilayered gate electrode comprising two layers or more of the above materials can be utilized. As shown in Fig. 9, for [For] example, a double layered structure comprising titanium silicide 901 formed on aluminum 902 or a double layered structure comprising aluminum 901 formed on titanium nitride 902 can be used. Each of the layers is provided at a thickness depending on the device characteristics.--

IN THE CLAIMS:

Please cancel claim 40 and amend claims 1, 6, 11, 16, 19 and 37 as follows:

1. (Amended) A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having at least one second thin film transistor formed over the substrate for driving said active matrix circuit, each of said first and second thin film transistors comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions of said second thin film transistor are overlapped with the gate electrode of said second thin film transistor;

wherein a distance between the channel forming region and the pair of first regions of said first thin film transistor is greater than that of said second thin film transistor.

6. (Amended) A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having at least one second thin film transistor formed over the substrate for driving said active matrix circuit, each of said first and second thin film transistors comprising:

gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions of said second thin film transistor are overlapped with the gate electrode of said second thin film transistor and a distance between the channel forming region and the pair of first regions in said first thin film transistor is within a range of 0.4 to 2 μm;

wherein a distance between the channel forming region and the pair of first regions of said first thin film transistor is greater than that of said second thin film transistor.

11. (Amended) A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having at least one second thin film transistor formed over the substrate for driving said active matrix circuit, each of said first and second thin film transistors comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

an insulating film comprising silicon oxide over the gate electrode;

wherein the pair of second regions of said second thin film transistor are overlapped with the gate electrode of said second thin film transistor and a distance between the channel forming region and the pair of first regions in said first thin film transistor is [different from] greater than that of said second thin film transistor.

16. (Amended) A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having an inverter circuit comprising at least a second and third thin film transistors formed over the substrate for driving said active matrix circuit, at least one of said second and third thin film transistors comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions are overlapped with the gate electrode of said second thin film transistor;

wherein a distance between the channel forming region and the pair of first regions of said first thin film transistor is greater than that of said second thin film transistor.

19. (Amended) A semiconductor device [including at least one thin film transistor, said thin film transistor] comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate;

a driving circuit having an inverter circuit comprising at least a second and third thin film transistors formed over the substrate for driving said active matrix circuit, at least one of said second and third thin film transistors comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is

smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions are overlapped with the gate electrode of said second thin film transistor and a distance between the channel forming region and the pair of first regions in said first thin film transistor is within a range of 0.4 to 2 μm;

wherein a distance between the channel forming region and the pair of first regions of said first thin film transistor is greater than that of said second thin film transistor.

37. (Amended) A semiconductor device comprising:

at least one first thin film transistor formed over a substrate;

a pixel electrode electrically connected to said first thin film transistor;

a driving circuit having at least one second thin film transistor formed over the substrate for driving first thin film transistor, each of said first and second thin film transistors comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a crystalline semiconductor film adjacent to said gate insulating film wherein said crystalline semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions of said second thin film transistors are overlapped with the gate electrode of said second thin film transistor;

wherein a distance between the channel forming region and the pair of first regions of said first thin film transistor is greater than that of said second thin film transistor.